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In How to create and use a sequence, we saw that a sequence calls on the tasks `start_item()` and `finish_item()`. You can avoid putting all these statements in your code by simply calling

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UVM sequence macros ``uvm_do` or ``uvm_do_with`. At compile time, these macros will be substituted with calls to `start_item()` and `finish_item()`. There are primarily four types of UVM macros that can be executed on the ...

How to use ``uvm_do` sequence macros

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SystemVerilog source code, do the following: add ./src to the include path on the command line, that is, +incdir+./.../src. add ./src/uvm_pkg.sv to the front of the list of files being compiled. add the following directives to your various SystemVerilog files.

From OVM to UVM: Getting Started with UVM

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generator creates project-specific boilerplate UVM code according to the Easier UVM guidelines.

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Starting Small to

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